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L2 same (gasket or interface)	13

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L2	L1 same fpga	65	L2
L1	embedded near3 (core or device)	10523	L1

END OF SEARCH HISTORY

L5: Entry 5 of 13 File: USPT May 11, 2004

DOCUMENT-IDENTIFIER: US 6735756 B1
TITLE: Method and architecture for dynamic device drivers

Detailed Description Text (5):
Referring to FIG. 2, a block diagram of a logical device driver instance 201 illustrating a common interface 205 and a virtual function table 211 pointing to a given version (220) of a device driver is shown. The hardware device and the device driver are preferably embedded in a Field Programmable Gate Array (FPGA) as contemplated in the present invention, but it should be understood that the device driver could also be external to the FPGA. A common interface 205 for the logical device driver instance 201 comprises a plurality of functions (206-209) linked to an embedded application 200. A virtual function table 211 comprises a plurality of function pointers (212-215) that point from each of the plurality of functions of the common interface (206-209) to the plurality of functions (221-224) corresponding to a specific version (220) of the device driver among a plurality of versions of the device driver.

Detailed Description Text (7):
Referring to FIG. 3, a block diagram of multiple logical device driver instances (301, 321, 331) of a device driver illustrating a shared common interface (303) and a virtual function table (305, 325, 335) for each instance pointing to a specific version (307 and 327, for example) of a device driver is shown. The hardware device and the device drivers are preferably embedded in a Field Programmable Gate Array (FPGA) as contemplated in the present invention, but it should be understood that the device drivers could also be external to the FPGA. A common interface 303 for the logical device driver instances comprises a plurality of functions linked to an embedded application 300. Each logical device driver instance, representing an instance of the hardware device, comprises a virtual function table (305, for example) that has pointers that point from each of the plurality of functions of the common interface 303 to functions corresponding to a specific version (307, for example) of the device driver among a plurality of versions (307 and 327, for example) of the device driver.

CLAIMS:

18. An FPGA-based system-on-chip (SoC), comprising: a hardware device embedded in the FPGA-based SoC; and a device driver instantiated in the FPGA and coupled to the hardware device, the device driver comprising: a common interface, wherein the common interface is common across a plurality of versions of the device driver and includes a plurality of functions linked to the hardware device; and a virtual function table that points from each of the plurality of functions of the common interface to a plurality of functions of a specific version of the device driver among the plurality of versions of the device driver, wherein a plurality of virtual function table pointers are set up during an initialization of the device driver.

L3: Entry 2 of 8 File: USPT Jan 4, 2005

DOCUMENT-IDENTIFIER: US 6839874 B1
TITLE: Method and apparatus for testing an embedded device

Brief Summary Text (8):
This presents a problem for testing the microprocessor core. Even if a microprocessor core were tested prior to FPGA fabrication, it would still need to be retested after such FPGA fabrication. To test such a microprocessor core, input and output pins of the combined FPGA and microprocessor core device need to be used to access internal pins of the microprocessor core device. However, the microprocessor core device may comprise more inputs and outputs than the device in which it is embedded. Moreover, extending inputs and outputs of the microprocessor core device to provide additional inputs and outputs of the combined device would necessitate significant additional interconnect routing and an increase in package size.

Detailed Description Text (3):
Referring to FIG. 1, there is shown a block diagram of an exemplary embodiment of a portion of an integrated circuit 100 comprising an FPGA 120 and an embedded microprocessor core 110 in accordance with one or more aspects of the present invention. Referring to FIG. 2, there is shown a block diagram of an exemplary embodiment of a test system 200 in accordance with one or more aspects of the present invention. With reference to FIGS. 1 and 2, conventionally a core, such as microprocessor core 110, is provided with test data vectors for testing such a core. These test data vectors may be programmed into a tester 202 for providing input test data vectors to integrated circuit 100 coupled via a printed circuit board 201. Conventionally tester 202 is a programmed computer having a motherboard. A daughter card, such as a "prototyping board" or "demonstration board," having a socket for receiving an integrated circuit 100 is plugged into a bus on the motherboard. A commercially available example of such a system is an AFX Silicon Verification System from Xilinx of San Jose, Calif. Alternatively, automatic test equipment may be used.

Detailed Description Text (6):
Prior to providing test data partial-vectors 203 to integrated circuit 100 for testing embedded core 110, FPGA 120, or more particularly a portion of FPGA 120, is programmed to provide vector controller 129. By programming FPGA 120 to provide vector controller 129, no additional circuitry is added for testing, rather existing programmable circuitry is used. Furthermore, FPGA 120 comprises sufficient connectivity or data width to and from embedded core 110 for purposes of testing. In other words, FPGA 120 may be interconnected to microprocessor core 110 via input conductive paths 111 and output conductive paths 112, where the number of conductive paths 111 is equal to the number of input pins 114-A used, and the number of conductive paths 112 is equal to the number of output pins 114-B used.

Detailed Description Text (10):
At step 303, registers for vector controller 129 are assigned. Registers may be used to receive and temporarily store respective partial test vector input from data_in and output for data_out. One or more cycle registers may be used to count input and output test vector information, such as partial test vectors and partial test vector results. Notably, as connectivity exists between vector controller 129

and embedded core 110, once FPGA 120 is configured, then there may be lingering signal or invalid data on metal lines interconnecting embedded core 110 and vector controller 129. Accordingly, it is important to delineate between valid data and such invalid data. Thus, vector controller 129 may be programmed with a state machine to make use of registers to determine: when valid assembled data is to be sent from vector controller 129 to embedded core 110, when valid core response data is to be sampled from embedded core 110 to vector controller 129, and when valid control output 121 and valid data output 122 is to be sent from vector controller 129 to tester 202.

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L4: Entry 1 of 1 File: USPT Aug 3, 2004

DOCUMENT-IDENTIFIER: US 6772405 B1
TITLE: Insertable block tile for interconnecting to a device embedded in an integrated circuit

Brief Summary Text (5):
Accordingly, when embedding a core, sometimes referred to as an embedded core, into an existing FPGA design, a portion of the FPGA layout is exchanged for layout of the embedded core. This is sometimes referred to as creating a "hole" in the "fabric" of the FPGA for insertion of an embedded core.

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US006772405B1

(12) **United States Patent**
Gan et al.

(10) **Patent No.: US 6,772,405 B1**
(45) **Date of Patent: Aug. 3, 2004**

(54) **INSERTABLE BLOCK TILE FOR INTERCONNECTING TO A DEVICE EMBEDDED IN AN INTEGRATED CIRCUIT**

(75) Inventors: **Andy H. Gan**, San Jose, CA (US); **Nigel G. Herron**, San Jose, CA (US)

(73) Assignee: **Xilinx, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 52 days.

(21) Appl. No.: **10/172,431**

(22) Filed: **Jun. 13, 2002**

(51) **Int. Cl.**[7] **G06F 17/50**

(52) **U.S. Cl.** **716/11**; 703/18; 714/738; 716/2; 716/12; 716/15

(58) **Field of Search** 703/18; 714/738; 716/2, 12, 15, 1, 6, 11, 17; 438/12

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,758,985	A	7/1988	Carter
4,855,669	A	8/1989	Mahoney
5,072,418	A	12/1991	Boutaud et al.
5,142,625	A	8/1992	Nakai
RE34,363	E	8/1993	Freeman
5,274,570	A	12/1993	Izumi et al.
5,311,114	A	5/1994	Sambamurthy et al.
5,339,262	A	8/1994	Rostoker et al.
5,347,181	A	9/1994	Ashby et al.
5,361,373	A	11/1994	Gilson

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP	0315275	A2	10/1989
EP	0 905 906	A2	3/1999
EP	1 235 351	A1	8/2002
WO	WO 93 25968	A1	12/1993

OTHER PUBLICATIONS

Sayfe Kiaei et al., "VLSI Design of Dynamically Reconfigurable Array Processor–Drap," IEEE, Feb. 1989, pp. 2484–2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016–5997.

Vason P. Srini, "Field Programmable Gate Array (FPGA) Implementation of Digital Systems: An Alternative to Asic," IEEE, May 1991, pp. 309–314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016–5997.

G. Maki et al., "A Reconfigurable Data Path Processor," IEEE, Aug. 1991, pp. 18–4.1 to 18–4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016–5997.

Jacob Davidson, "FPGA Implementation of Reconfigurable Microprocessor," IEEE, Mar. 1993, pp. 3.2.1–3.2.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016–5997.

Christian Iseli et al., "Beyond Superscaler Using FPGA's," IEEE, Apr. 1993, pp. 486–490, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016–5997.

P.C. French et al., "A Self–Reconfiguring Processor,"; IEEE, Jul. 1993, pp. 50–59, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016–5997.

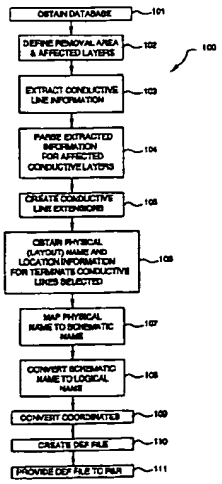
(List continued on next page.)

Primary Examiner—Thuan Do
(74) *Attorney, Agent, or Firm*—W. Eric Webostad

(57) **ABSTRACT**

Method and apparatus for an insertable block tile is described. More particularly, a reserved area in an integrated circuit layout is removed, and terminated conductive line information is extracted from a layout database affected by the removal. The terminated conductive line information is used to create extensions or pins of the conductive lines terminated, as well as to identify signals associated with those terminated conductive lines. These physical or layout names and coordinates are mapped and then translated to logic names and coordinates for placement and routing to create the insertable block tile.

19 Claims, 5 Drawing Sheets



US006772405B1

(12) **United States Patent**
Gan et al.

(10) **Patent No.: US 6,772,405 B1**
(45) **Date of Patent: Aug. 3, 2004**

(54) **INSERTABLE BLOCK TILE FOR INTERCONNECTING TO A DEVICE EMBEDDED IN AN INTEGRATED CIRCUIT**

(75) Inventors: **Andy H. Gan**, San Jose, CA (US); **Nigel G. Herron**, San Jose, CA (US)

(73) Assignee: **Xilinx, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 52 days.

(21) Appl. No.: **10/172,431**

(22) Filed: **Jun. 13, 2002**

(51) **Int. Cl.**[7] **G06F 17/50**

(52) **U.S. Cl.** **716/11**; 703/18; 714/738; 716/2; 716/12; 716/15

(58) **Field of Search** 703/18; 714/738; 716/2, 12, 15, 1, 6, 11, 17; 438/12

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,758,985	A	7/1988	Carter
4,855,669	A	8/1989	Mahoney
5,072,418	A	12/1991	Boutaud et al.
5,142,625	A	8/1992	Nakai
RE34,363	E	8/1993	Freeman
5,274,570	A	12/1993	Izumi et al.
5,311,114	A	5/1994	Sambamurthy et al.
5,339,262	A	8/1994	Rostoker et al.
5,347,181	A	9/1994	Ashby et al.
5,361,373	A	11/1994	Gilson

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP	0315275	A2	10/1989
EP	0 905 906	A2	3/1999
EP	1 235 351	A1	8/2002
WO	WO 93 25968	A1	12/1993

OTHER PUBLICATIONS

Sayfe Kiaei et al., "VLSI Design of Dynamically Reconfigurable Array Processor–Drap," IEEE, Feb. 1989, pp. 2484–2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016–5997.

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Jacob Davidson, "FPGA Implementation of Reconfigurable Microprocessor," IEEE, Mar. 1993, pp. 3.2.1–3.2.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016–5997.

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P.C. French et al., "A Self–Reconfiguring Processor,"; IEEE, Jul. 1993, pp. 50–59, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016–5997.

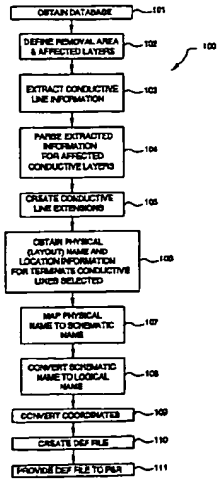
(List continued on next page.)

Primary Examiner—Thuan Do
(74) *Attorney, Agent, or Firm*—W. Eric Webostad

(57) **ABSTRACT**

Method and apparatus for an insertable block tile is described. More particularly, a reserved area in an integrated circuit layout is removed, and terminated conductive line information is extracted from a layout database affected by the removal. The terminated conductive line information is used to create extensions or pins of the conductive lines terminated, as well as to identify signals associated with those terminated conductive lines. These physical or layout names and coordinates are mapped and then translated to logic names and coordinates for placement and routing to create the insertable block tile.

19 Claims, 5 Drawing Sheets



US006735756B1

(12) **United States Patent**
Linn et al.

(10) **Patent No.: US 6,735,756 B1**
(45) **Date of Patent: May 11, 2004**

(54) **METHOD AND ARCHITECTURE FOR DYNAMIC DEVICE DRIVERS**

(75) Inventors: **John H. Linn**, Albuquerque, NM (US); **Richard P. Moleres**, Albuquerque, NM (US)

(73) Assignee: **Xilinx, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 119 days.

(21) Appl. No.: **10/082,436**

(22) Filed: **Feb. 22, 2002**

(51) **Int. Cl.**[7] **G06I 17/50**
(52) **U.S. Cl.** **716/16**; 716/1; 716/3
(58) **Field of Search** 716/16, 1–3; 709/321, 709/327, 223; 717/140, 148, 70; 710/33

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,361,373	A		11/1994	Gilson
5,537,601	A		7/1996	Kimura et al.
5,652,904	A		7/1997	Trimberger
5,671,355	A		9/1997	Collins
5,752,035	A		5/1998	Trimberger
5,970,254	A		10/1999	Cooke et al.
6,020,755	A		2/2000	Andrews et al.
6,096,091	A		8/2000	Hartmann
6,279,045	B1		8/2001	Muthujumaraswathy et al.
6,282,627	B1		8/2001	Wong et al.
6,292,855	B1	*	9/2001	Johnson et al. 710/33
6,343,207	B1		1/2002	Hessel et al.
6,393,495	B1	*	5/2002	Flory et al. 709/327
6,434,742	B1	*	8/2002	Koepele, Jr. 717/140
6,473,824	B1	*	10/2002	Kreissig et al. 348/222.1
6,477,643	B1	*	11/2002	Vorbach et al. 713/100
6,522,167	B1	*	2/2003	Ansari et al. 326/39
2002/0112227	A1	*	8/2002	Kramskoy et al. 717/148
2002/0178243	A1	*	11/2002	Collins 709/223
2003/0048473	A1	*	3/2003	Rosen 358/1.15
2003/0088866	A1	*	5/2003	Boldon et al. 717/170
2003/0101290	A1	*	5/2003	Lin et al. 709/327
2003/0135663	A1	*	7/2003	Duncan et al. 709/321
2003/0145127	A1	*	7/2003	Unice 709/321

OTHER PUBLICATIONS

Cary D. Snyder and Max Baron; "Xilinx's A-to-Z System Platform"; Cahners Microprocessors; The Insider's Guide to Microprocessor Hardware; Microdesign Resources; Feb. 6, 2001; pp. 1–5.

* cited by examiner

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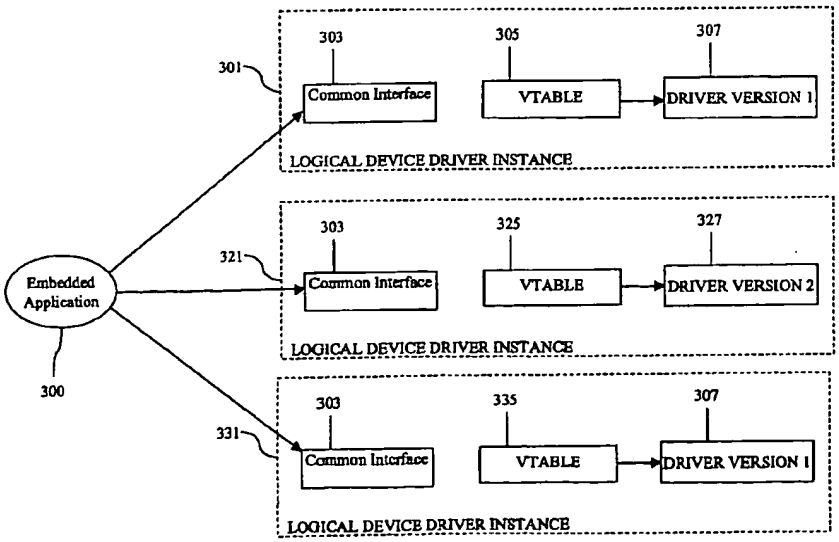
Assistant Examiner—Magid Y. Dimyan
(74) *Attorney, Agent, or Firm*—Pablo Meles; Lois D. Cartier

(57) **ABSTRACT**

In a plurality of logical device driver instances, each instance **(201)** representing a specific version **(220)** of the device driver, can be accessed by an embedded application **(200)** via a common interface **(205)**. A logical device driver instance includes the common interface which includes a plurality of functions **(206–209)** linked to the embedded application. A logical device driver also includes a virtual function table **(211)** having pointers **(212–215)** that points from each of the plurality of functions of the common interface to a plurality of functions **(221–224)** of a specific version of the device driver among a plurality of versions of the device driver. The virtual function table is set up dynamically during run-time initialization of a logical device driver instance.

28 Claims, 3 Drawing Sheets



US006839874B1

(12) **United States Patent**
Fang

(10) **Patent No.: US 6,839,874 B1**
(45) **Date of Patent: Jan. 4, 2005**

(54) **METHOD AND APPARATUS FOR TESTING AN EMBEDDED DEVICE**

(75) Inventor: **Ying Fang**, San Jose, CA (US)

(73) Assignee: **Xilinx, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 498 days.

(21) Appl. No.: **10/086,130**

(22) Filed: **Feb. 28, 2002**

(51) **Int. Cl.**[7] **G06F 11/00**
(52) **U.S. Cl.** **714/738**; 714/30; 714/724; 714/725
(58) **Field of Search** 714/738, 724, 714/725, 30, 47, 48, 734, 733

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,758,985	A		7/1988	Carter
4,855,669	A		8/1989	Mahoney
5,072,418	A		12/1991	Boutaud et al.
5,142,625	A		8/1992	Nakai
RE34,363	E		8/1993	Freeman
5,274,570	A		12/1993	Izumi et al.
5,311,114	A		5/1994	Sambamurthy et al.
5,339,262	A		8/1994	Rostoker et al.
5,347,181	A		9/1994	Ashby et al.
5,361,373	A		11/1994	Gilson
5,457,410	A		10/1995	Ting
5,473,267	A		12/1995	Stansfield
5,500,943	A		3/1996	Ho et al.
5,504,738	A		4/1996	Sambamurthy et al.
5,537,601	A		7/1996	Kimura et al.
5,543,640	A		8/1996	Sutherland et al.
5,550,782	A		8/1996	Cliff et al.
5,553,082	A	*	9/1996	Connor et al. 714/733
5,574,930	A		11/1996	Halverson, Jr. et al.
5,574,942	A		11/1996	Colwell et al.
5,581,745	A		12/1996	Muraoka
5,600,845	A		2/1997	Gilson
5,652,904	A		7/1997	Trimberger
5,671,355	A		9/1997	Collins
5,705,938	A		1/1998	Kean
5,732,250	A		3/1998	Bates et al.
5,737,631	A		4/1998	Trimberger
5,740,404	A		4/1998	Baji
5,742,179	A		4/1998	Sasaki
5,742,180	A		4/1998	DeHon et al.

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP	0315275	A2	10/1989
EP	0 905 906	A2	3/1999
EP	1 235 351	A1	8/2002
WO	WO 93 25968	A1	12/1993

OTHER PUBLICATIONS

U.S. patent application Ser. No. 10/043,769, Schulz, filed Jan. 9, 2002.

(List continued on next page.)

Primary Examiner—Phung M. Chung
(74) *Attorney, Agent, or Firm*—H. C. Chan

(57) **ABSTRACT**

Method and apparatus for testing a device embedded in a programmable logic device is described. Because an embedded device, such as a microprocessor core, comprises more input and output pins than a programmable logic device, such as a field programmable gate array, in which it is located, providing a test vector wider than the number of external input and output pins of the programmable logic device is problematic. To solve this problem, at least a portion of the programmable logic device is programmed to function as a vector controller, where a test vector may be provided to the vector controller in sections, reassembled by the vector controller and provided to the embedded device after reassembly. Moreover, a test vector result in response to the test vector input is obtained by the vector controller and sectioned for outputting.

20 Claims, 6 Drawing Sheets